METHOD AND APPARATUS FOR PROVIDING DEBUG FUNCTIONALITY IN A BUFFERED MEMORY CHANNEL

ABSTRACT OF THE DISCLOSURE

Some embodiments of the invention enable debugging functionality for memory devices residing on a memory module that are buffered from the memory bus by a buffer chip. Some embodiments map connector signals from a tester coupled to the high speed interface between the buffer chip and the memory bus to an interface between the buffer chip and the memory devices. During test mode, some embodiments bypass the normal operational circuitry of the buffer chip and provide a direct connection to the memory devices. Other embodiments use the existing architecture of the buffer chip to convert high speed pins into low speed pins and map them to pins that are connected to the memory devices. Other embodiments are described in the claims.